Notice of Allowability	Application No.	Applicant(s)	
	10/028,667	CHOI ET AL.	
	Examiner	Art Unit	
	Matthew Landau	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the response filed July 29, 2005*.

2. ☒ The allowed claim(s) is/are *1,2,5-9,11,12,14 and 22*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Robert Webster (Reg. #46,472) on October 12, 2005.

Please amend the claims as follows:

1. (Currently Amended) An array substrate for a liquid crystal display device, comprising:

a substrate;

gate and data lines crossing each other on the substrate;

a thin film transistor connected to the gate and data lines, the thin film transistor having a gate electrode, a semiconductor layer, and source and drain electrodes facing and spaced apart from each other;

a passivation layer over the gate and data lines and the thin film transistor, the passivation layer having a contact hole exposing a portion of a side edge surface of the drain electrode;

a gate insulation layer formed underneath the passivation layer, wherein the contact hole is defined through the passivation layer and the gate insulation layer;

a pixel electrode on the passivation layer;

and a storage capacitor including a portion of the gate line as a first storage electrode, a portion of the gate insulation layer, and second storage electrode having an island shape, wherein the second storage electrode is disposed directly contacting the gate insulation layer.

6. (Currently Amended) An array substrate for a liquid crystal display device, comprising:

a substrate;

gate and data lines crossing each other on the substrate;

a thin film transistor connected to the gate and data lines, the thin film transistor having a gate electrode extending from the gate line, a semiconductor layer, a first ohmic contact layer, a second ohmic contact layer, and source and drain electrodes, the semiconductor layer having an end aligned with and directly below an end of the source electrode, the semiconductor layer having an opposite end aligned with and directly below an end of the drain electrode;

a passivation layer pattern on the drain line and the thin film transistor, the passivation layer pattern exposing a portion of a side edge surface of the drain electrode, and

a pixel electrode connected to the drain electrode; and

a gate insulation film formed over the gate line, wherein a portion of the pixel electrode is formed directly on the gate insulation film at a pixel region defined by the gate and data lines.

Allowable Subject Matter

Claims 1, 2, 5-9, 11, 12, 14, and 22 are allowed.

The following is an examiner's statement of reasons for allowance:

Regarding claim 1, the prior art of record, either singularly or in combination, does not disclose or suggest the combination of limitations including a contact hole exposing a portion of a side edge surface of the drain electrode, and a storage capacitor including a portion of the gate line as a first storage electrode, a portion of the gate insulation layer, and a second storage electrode having an island shape, wherein the second storage electrode is disposed directly contacting the gate insulation layer.

Regarding claim 6, the prior art of record, either singularly or in combination, does not disclose or suggest the combination of limitations including the passivation layer pattern exposing a portion of a side edge surface of the drain electrode.

Regarding claim 12, the prior art of record, either singularly or in combination, does not disclose or suggest the combination of limitations including wherein the pixel electrode contacts side portions of the semiconductor layer and one of the first and second ohmic contact layers. Note that Applicant's response filed July 29, 2005 has established that the Kwak patent (used in the previous rejection of claim 12) was commonly assigned to the assignee of this application (see page 11 of the Remarks section).

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew C. Landau whose telephone number is (571) 272-1731.

The examiner can normally be reached from 8:30 AM - 5:30 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone numbers for the organization where this application or proceeding is assigned are (571) 273-8300 for regular communications and (571) 273-8300 for After Final communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should any questions arise regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER

Matthew C. Landau

October 12, 2005